B4BQDD8CXXXC-XX0

400GbE QSFP-DD Active Optical Cable (AOC)

Description

B4BQDD8CXXXC-XX0 is 400Gb/s QSFP-DD active optical cable (AOC). It is compliant with the QSFP-DD MSA Rev5.0 and IEEE 802.3bs, and Common Management Interface Specification Rev4.0. 400G AOC is an assembly of eight full-duplex lanes, where each lane is capable of transmitting data at rates up to 53.125Gb/s PAM-4.

Features

- Data rate up to 425Gbps (8x PAM4 26.5625 GBd)
- High speed I/O electrical interface (400GAUI-8)
- I2C interface with integrated Digital Diagnostic monitoring
- 850nm VCSEL laser and PIN receiver
- QSFP-DD MSA compliant
- Single +3.3V power supply
- Power consumption (Each end) <8 W
- Operating case temperature 0 to 70 ºC
- CMIS 4.0 management interface

Applications

- Data Center
- Switch/Router interconnections

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1 FUNCTIONAL DESCRIPTION

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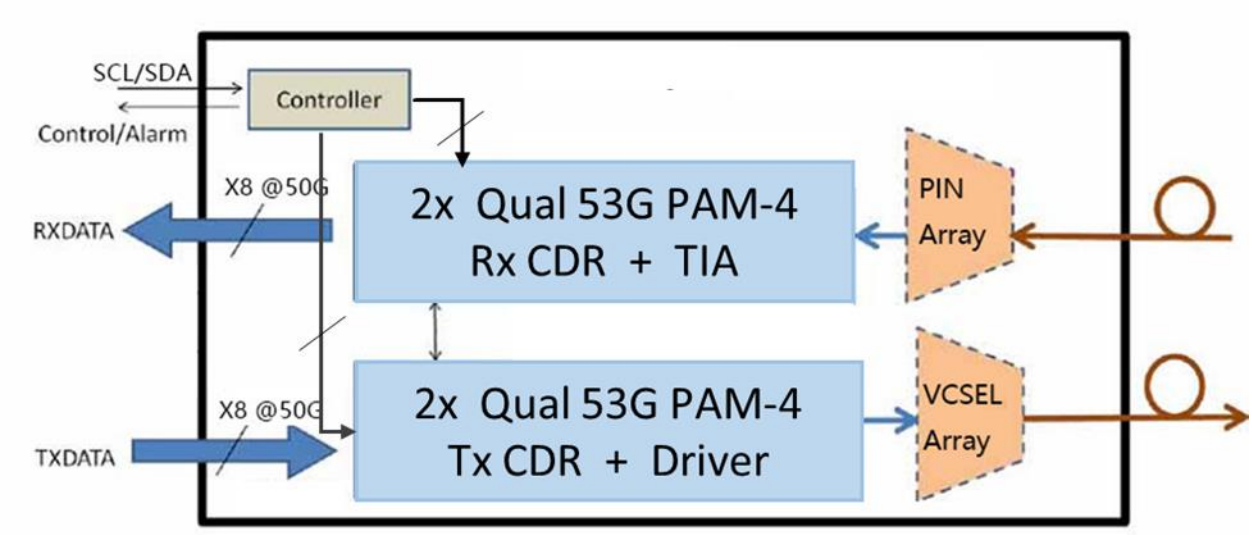

Figure 1 Functional Block Diagram

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2 PERFORMANCE SPECIFICATIONS

2.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Table 1 Absolute Maximum Ratings

No.	Parameter	Symbol	Min.	Max.	Unit	Remarks
1	Supply Voltage	Vcc	0	+3.6	V	
2	Storage Temperature		-40	85	°C	
3	Operating Relative Humidity	RH	15	85	%	

2.2 Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Table 2 Operating Environment

No	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Voltage	Vcc	3.135	3.3	3.465	V	
2	Supply Voltage Noise Tolerance	PSNR	-	-	66	mV	10 Hz –10 MHz
3	Power Consumption	P_4	-	-	8	W	Each end
4	Instantaneous peak current	Icc_ip_4			3200	mA	
5	Sustained peak current	Icc-sp_4			2640	mA	
6	Supply Current	Icc-4	--	-	2551.8	mA	Steady state
7	Case Temperature	T_C	0	25	70	°C	
8	Lane Bit Rate	BR_{LANE}		53.125		Gb/s	
9	Signaling Speed Accuracy	SSA	-100		100	Ppm	
10	BER				2.4E-4		Pre-FEC

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2.3 Electrical Interface

Table 3 Electrical Characteristics

No.	Parameter	Min.	Typ.	Max.	Unit	Remarks
Module output (each lane, at TP4) [Note 1]						
1	Signaling rate per lane (range)	-100ppm	26.5625	+100ppm	GBd	
2	AC Common-mode output voltage (RMS)	-	-	17.5	mV	
3	Differential peak-to-peak output voltage	-	-	900	mV	
4	Near-end ESMW (Eye symmetry mask width)	0.265	-	-	UI	
5	Near-end Eye height, differential	70			mV	
6	Far-end ESMW (Eye symmetry mask width)	0.2	-	-	UI	
7	Far-end Eye height, differential	30	-	-	mV	
8	Far-end pre-cursor ISI ratio	-4.5	-	2.5	%	
9	Differential output return loss	Equation (83E-2)	-	-	dB	Note 2
10	Common to differential mode conversion return loss	Equation (83E-3)	-	-	dB	Note 2
11	Differential termination mismatch	-	-	10	%	
12	Transition time (20% to 80%)	9.5	-	-	ps	
13	DC common mode voltage	-350	-	2850	mV	
Module input (each lane)						
1	Signaling rate per lane (range)	-100ppm	26.5625	+100ppm	GBd	
2	Differential pk-pk input voltage tolerance	900	-	-	mV	at TP1a
3	Differential input return loss	Equation (83E-5)	-	-	dB	at TP1, Note 2
4	Differential to common mode input return loss	Equation (83E-6)	-	-	dB	at TP1, Note 2
5	Differential termination mismatch	-	-	10	%	at TP1
6	ESMW (Eye symmetry mask width)	0.22	-	-	UI	at TP1a
7	Eye width	0.22	-	-	UI	at TP1a
8	Applied pk-pk sinusoidal jitter	Table 120E–6			MHz, UI	at TP1a
9	Eye height	32	-	-	mV	at TP1a

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10	Single-ended input voltage tolerance range	-0.4	-	3.3	V	at TP1a
11	DC common mode voltage	-350	-	2850	mV	at TP1

Note 1: Electrical module output is squelched for loss of optical input signal.

Note2: IEEE Std 802.3-2018 Section 6

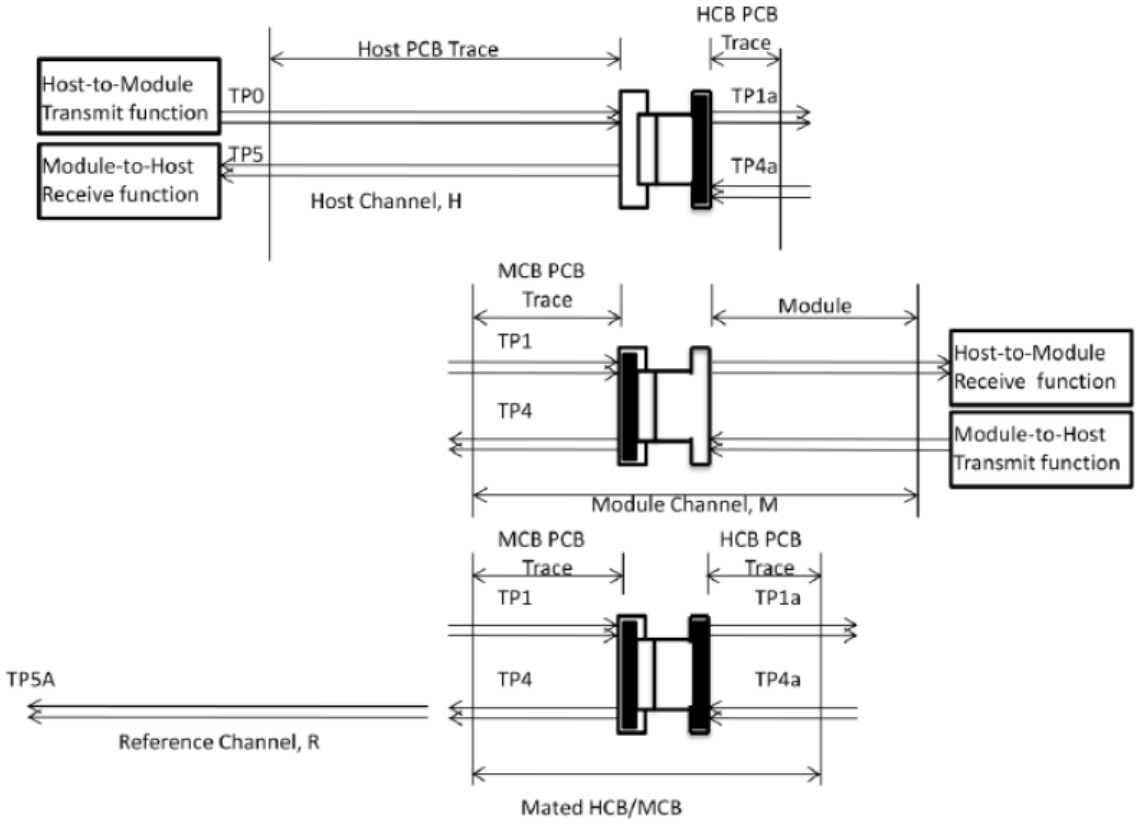

Figure 2 Reference Test Points

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3 HIGH SPEED DATA INTERFACE

3.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP-DD module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC. The QSFP-DD module host interface is internally AC coupled, so AC-coupling is not required on the host PCB.
Output squelch for loss of optical input signal (RX Squelch) is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output. In the squelched state, output impedance levels are maintained, while the differential voltage amplitude shall be less than 50 mVpp.

3.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP-DD optical module. The AC coupling is implemented inside the QSFP-DD optical module and not required on the Host board.
Output squelch for loss of electrical signal (Tx Squelch) is an optional function. Where implemented, it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.
For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

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4 CONTROL INTERFACE

4.1 Low Speed Control Pins

In addition to the 2-wire serial interface the transceiver has the following low speed signals for control and status: LPMode, ResetL, ModSel, IntL and ModPrsL. See the QSFP-DD MSA Hardware Specification for detailed descriptions of each signal.

4.2 Low Speed Electrical Specifications

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc.

Table 4 Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL (max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3 kohm pullup resistor, max. For 1000 kHz clock rate refer to Figure 6 in QSFPDD MSA HW Spec [3].
	Cb		200	pF	For 400 kHz clock rate use 1.6 kohm pullup resistor, max. For 1000 kHz clock rate refer to Figure 6 in QSFPDD MSA HW Spec [3].
LPMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
	VOH	Vcc-0.5	Vcc+0.3	V	10 kohm pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL= 2.0mA

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	VOH	Vcc-0.5	Vcc+0.3	V	ModPrsL can be implemented as a short-circuit to GND on the module

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4.3 2-Wire Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. This QSFP-DD specification is based on SFF-8636 but with modifications to support an 8-channel module, and as such is not directly backwards compatible with SFF-8636. Byte 00 on the Lower Page or Address 128 Page 00 is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map.

The QSFP-DD Module supports alarm, control and monitor functions via a two-wire interface bus. Upon module initialization, these functions are available. QSFP-DD two-wire electrical interface consists of 2 pins of SCL (2-wire serial interface clock) and SDA (2-wire serial interface data). The low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. The timing requirements on the two-wire interface are listed in Table 7 and Figure 4.

Table 5 Management Interface Timing

Parameter	Symbol	Fast Mode Plus (1 MHz)		Unit	Conditions
		Min	Max		
Clock Frequency	fSCL	0	1000	kHz	
Clock Pulse Width Low	tLOW	0.50		μs	
Clock Pulse Width High	tHIGH	0.26		μs	
Time bus free before new transmission can start	tBUF	1		μs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.26		μs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.26		μs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		μs	
Data In Setup Time	tSU.DAT	0.1		μs	
Input Rise Time	tR		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc), see Figure 6 in QSFPDD MSA HW Spec [3].

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Parameter	Symbol	Fast Mode Plus (1 MHz)		Unit	Conditions
		Min	Max		
Input Fall Time	tF		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc), in QSFPDD MSA HW Spec [3]
STOP Setup Time	tSU.STO	0.26		μs	
STOP Hold Time	tHD.STO	0.26		us	
Aborted sequence bus release	Deselect _Abort		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time[1]	tSU.ModSelL	2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence. (Target)
ModSelL Hold Time[1]	tHD.ModSelL	2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status. (Target)
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500	us	Time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non-volatile registers	tWR		80	ms	Time to complete a Single or Sequential Write to non-volatile registers.
Accept a single or sequential write to volatile memory.	tNACK		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50k		cycles	Module Case Temperature= 70 °C (Target)

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Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.

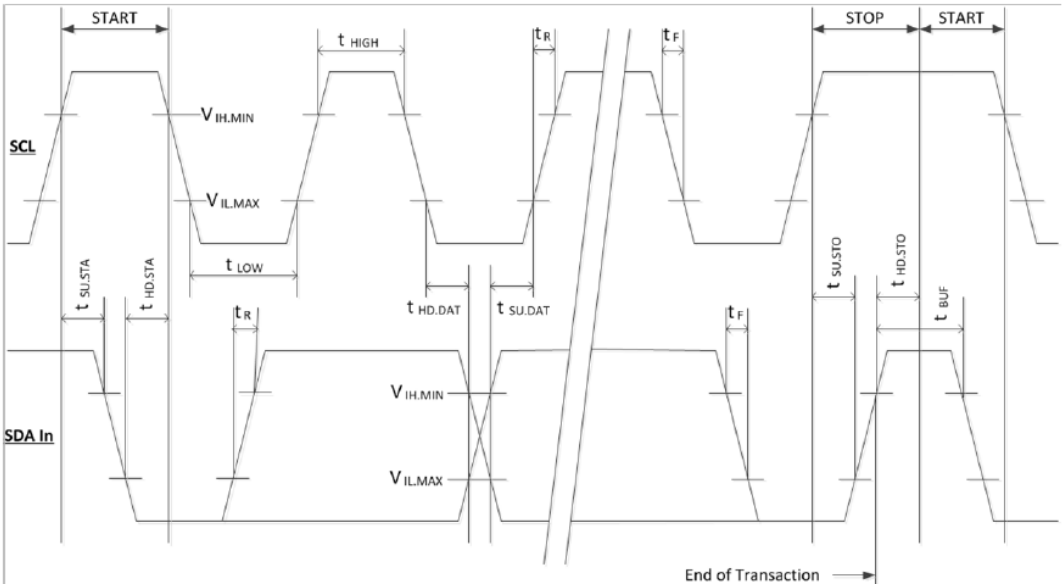

Figure 3 2-Wire Interface Timing Diagram

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4.4 Soft Control and Status Functions

Table 8 lists the required timing performance for software control and status functions.

Table 6 Control and Status Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1], hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	10		μs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
IntL Deassert Time	toff_IntL		500	μs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[3] until associated IntL assertion is inhibited.
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes.

Note 1: Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 2.

Note 2: Measured from the rising edge of SDA in the stop bit of the read transaction.

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Note 3: Measured from the rising edge of SDA in the stop bit of the write transaction.

Note 4: Rx LOS condition is defined at the optical input by the relevant standard.

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4.5 Squelch and Disable Assert/De-assert and Enable/Disable Timing

Table 7 I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached,
Tx Squelch De-assert Time	toff_Txsq	5 (Tentative)	s	Tx squelch deassert is system and implementation dependent.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence[1] until optical output falls below 10% of nominal.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	Not applicable (Optional fast mode not supported)		Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal and see notes 2 and 3.
Tx Disable De-assert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal and see note 2.
Tx Disable De-assert Time (optional fast mode)	toff_txdisf	Not applicable (Optional fast mode not supported)		Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see note 3.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable De-assert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis	Not applicable (Tx/Rx Auto Squelch Disable not supported)		This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable De-assert Time	toff_sqdis	Not applicable (Tx/Rx Auto Squelch Disable not supported)		This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.

Note 1: Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.

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Note 2. CMIS 4.0 and beyond the listed values are superseded by the advertised DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in P01h.168.

Note 3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times (P01h.168) that can be advertised by such modules (for CMIS 4.0 and beyond).

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5 POWER

The power supply has six designated pins, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. Vcc1 and Vcc2 are used to supplement VccTx, VccTx1, VccRx or VccRx1 at the discretion of the module vendor. Power is applied concurrently to these pins.

A host board together with the QSFP-DD module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 2 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

QSFP56-DD modules are categorized into several power classes as listed in Table 10. The power class of AD2H00ENA is class 04.

Table 8 Maximum Power Classes

Power Class	Max Power (W)
1	1.5
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

5.1 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 5.

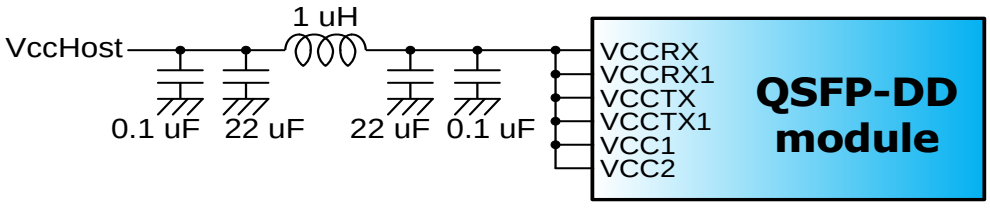

Figure 4 Recommended Host Board Power Supply Filtering

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Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP-DD modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted, the module will proceed to High Power Mode without host intervention. Figure 6 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 2.

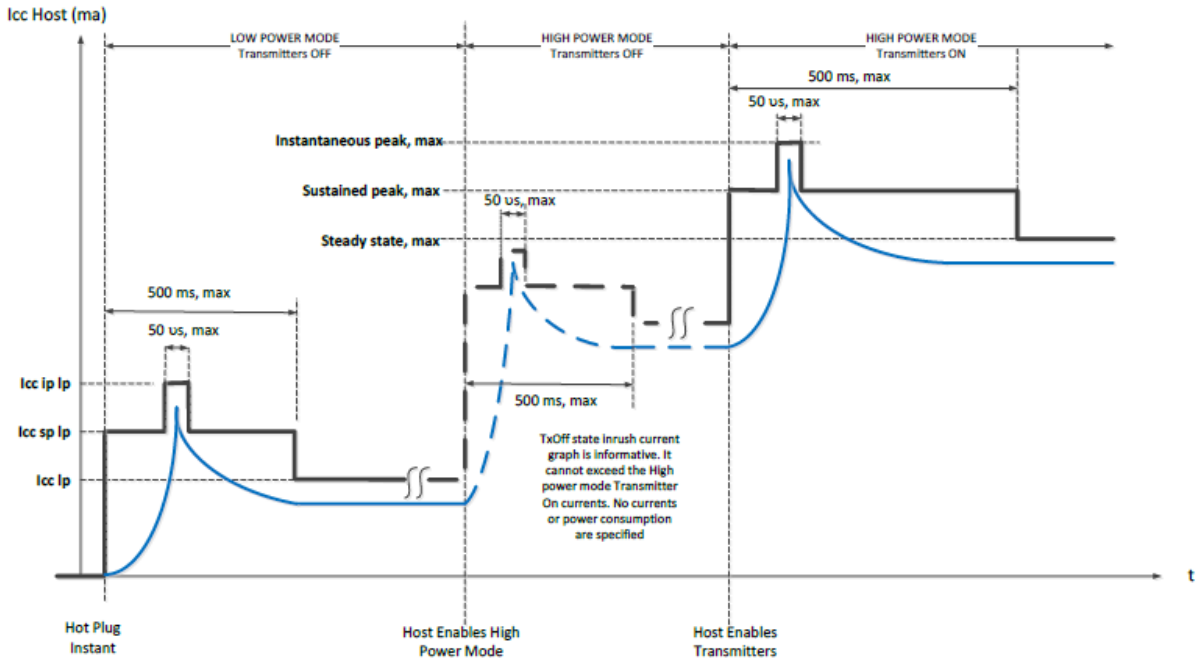

Figure 5 Instantaneous and Sustained Peak Currents for Icc Host

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6 PIN ASSIGNMENT

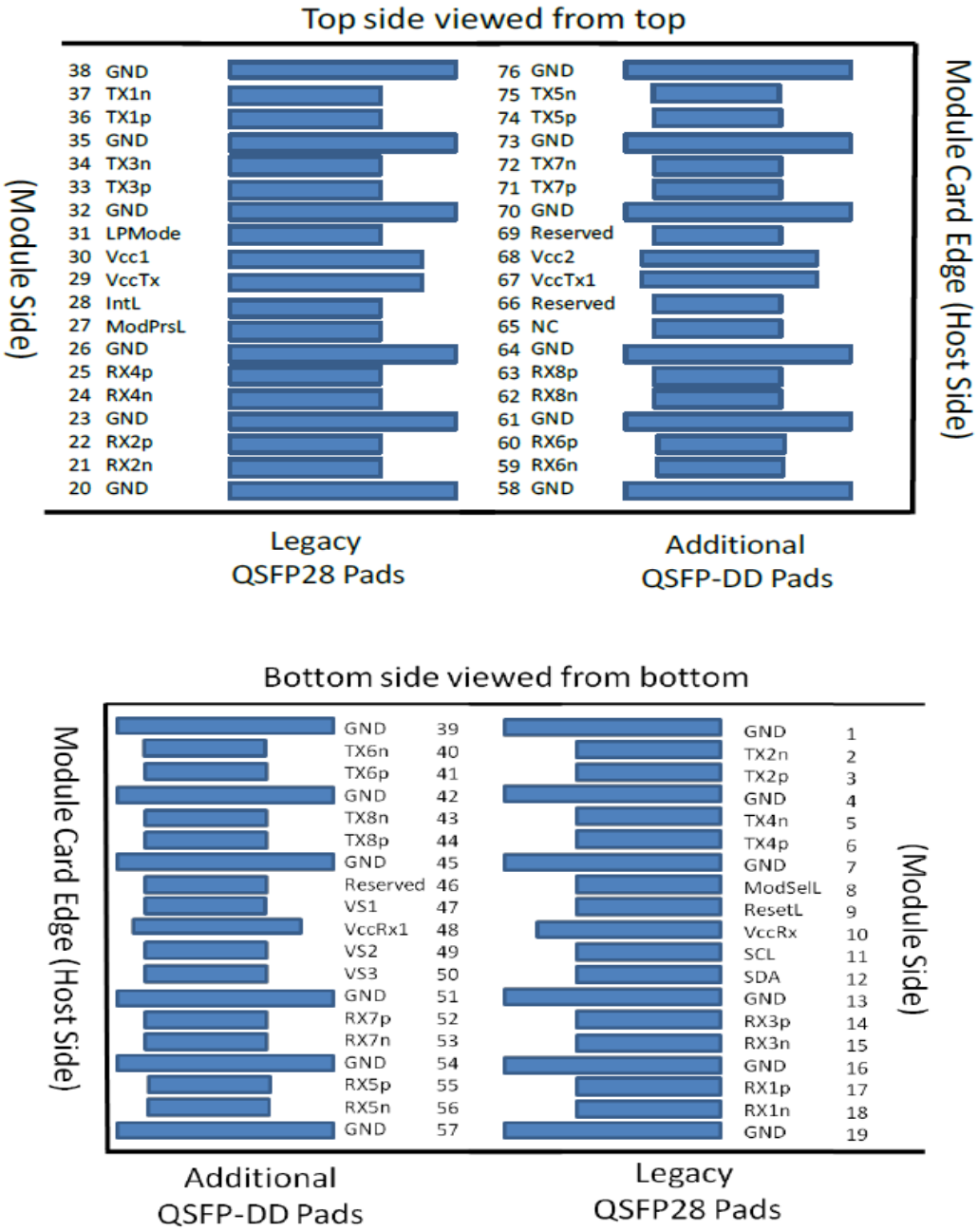

Figure 6 Module Pads

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Table 9 Pin Description

Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL	Interrupt.	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2

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Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	No connect	3A	3
47		NC	No connect	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		NC	No connect	3A	
50		NC	No connect	3A	
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1

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Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	No Connect	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	No Connect	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

[1] QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

[3] All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

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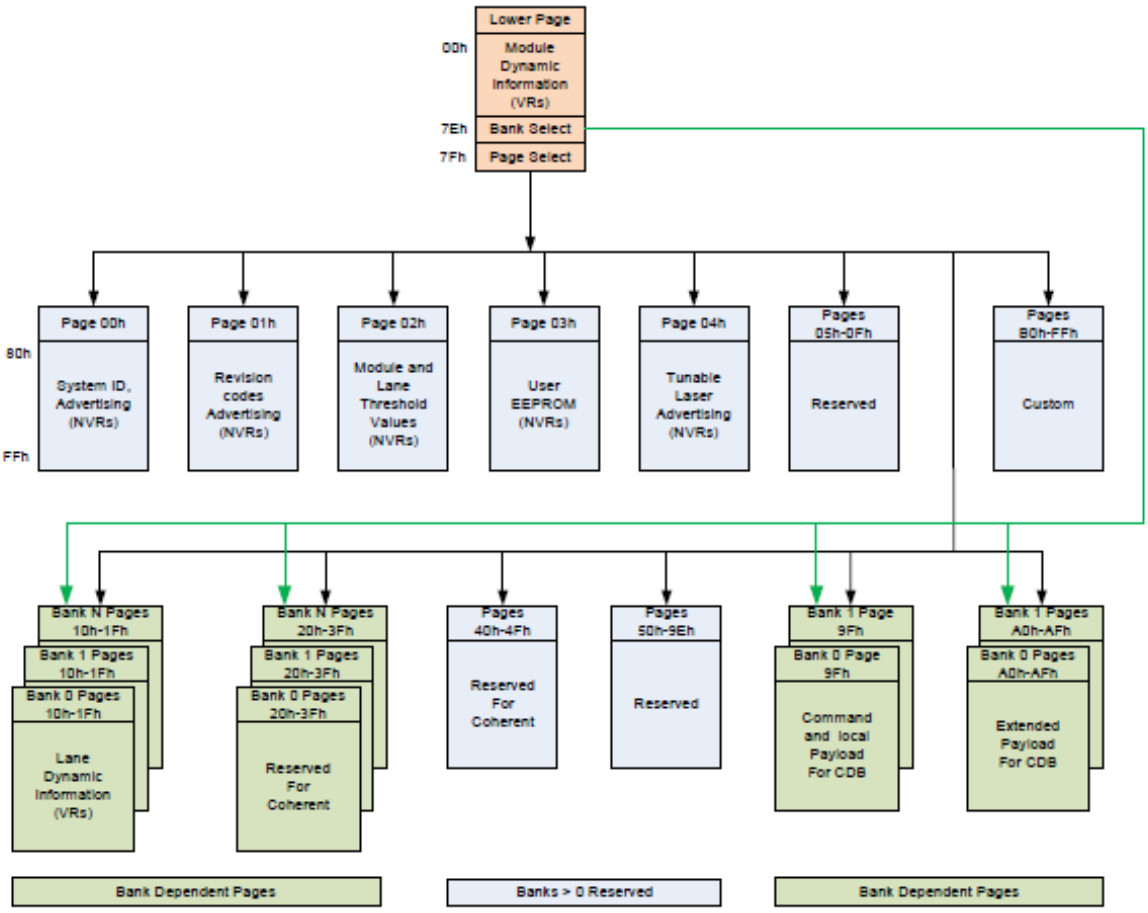
7 DIGITAL DIAGNOSTIC MEMORY MAP



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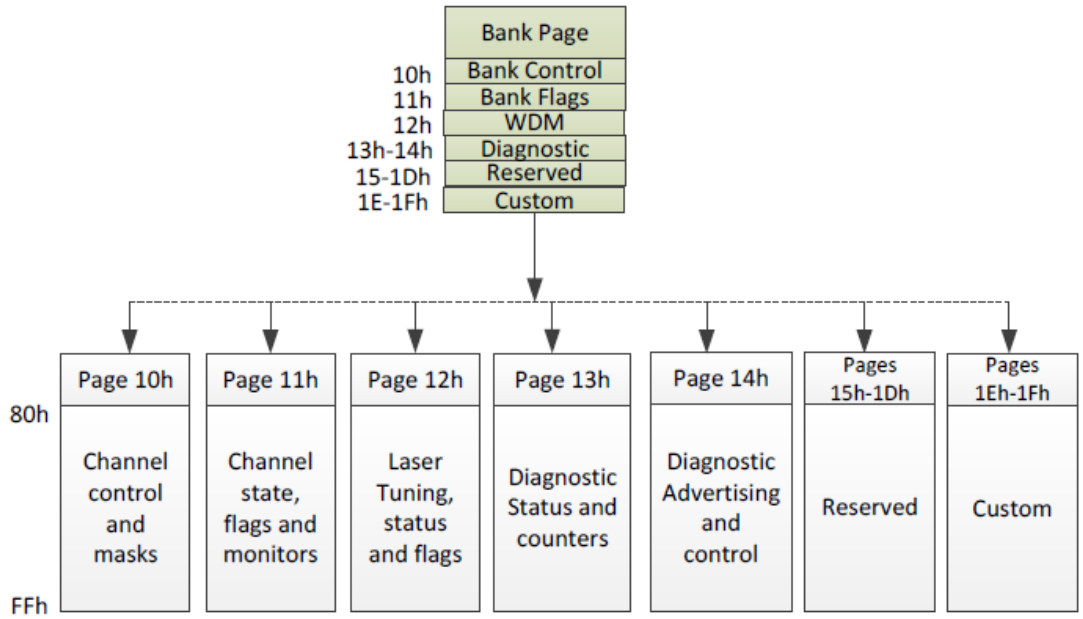

Table 10 Digital Diagnostic Monitor Accuracy

No.	Parameter	Symbol	Accuracy	Unit	Remarks
1	Transceiver Case Temperature absolute error	DMI_TEMP	±3	℃	Over operating temp
2	Supply voltage monitor absolute error	DMI _VCC	±3%	V	Full operating range
3	Channel Bias current monitor	DMI_IBIAS	±3%	mA	Per channel
4	Channel RX power monitor absolute error	DMI_RX	±3	dB	Per channel
5	Channel TX power monitor absolute error	DMI_TX	±3	dB	Per channel

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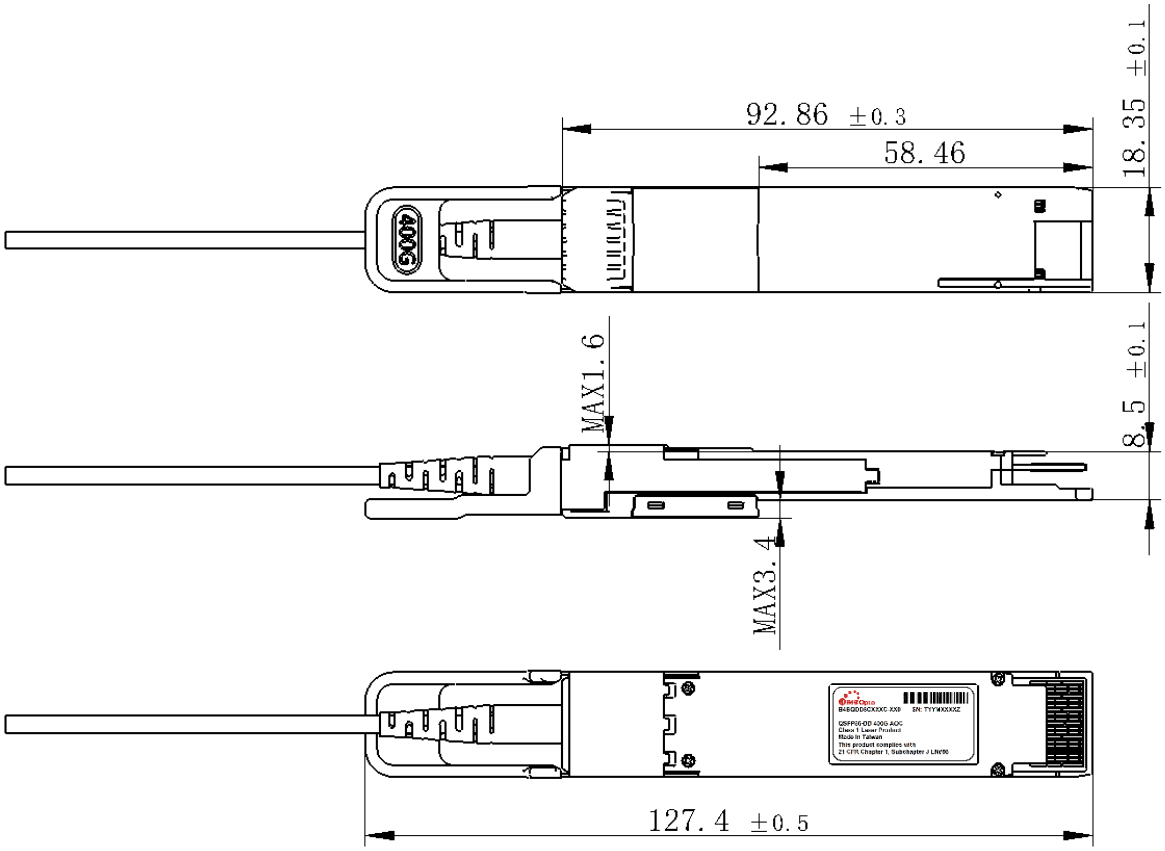
8 MECHANICAL DIMENSIONS

Unit: mm



Pull tab color: Beige

Figure 7 Mechanical Dimensions

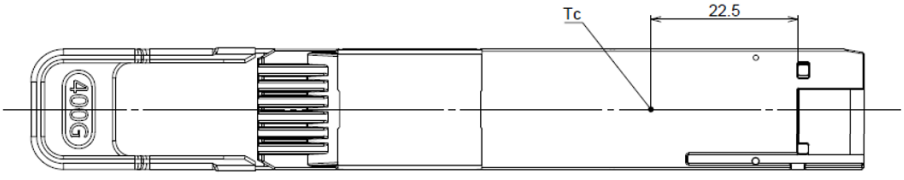


Figure 8 Case temperature measurement point

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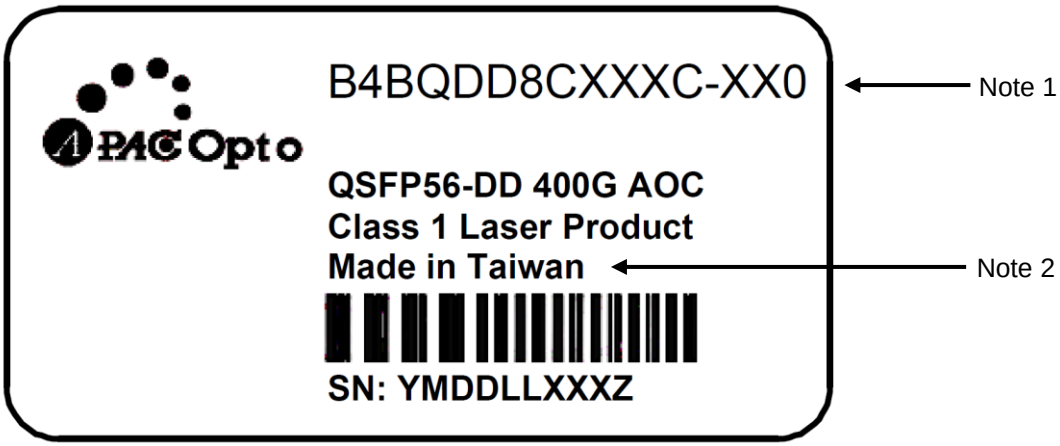
9 LABEL DESIGNS

27.7 mm x 15.7 mm



Notes:

Note 1	Serial Number	YMDDLLXXXZ (ex. NC2501001A) Y: year of manufactured (ex. 9 = 2009, A = 2010, …, N = 2023, …) M: Month of manufactured (1~9 for Jan.~Sep., A for Oct., B for Nov., C for Dec.) DD: Day of manufactured LL: Last 2 codes of APAC manufacture order sequency number XXX: Running number (3 digits sequential number from 001 to 999) Z: A for one end of the AOC and B for another end of module.
Note 2	Manufacture Location	Made in Taiwan

Figure 9 Component Label

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10 REGULATORY COMPLIANCE

Certification	Standard
EMC/EMI	FCC Part 15, Subpart B (Class B) EN55032 (Class B)
ESD	EN61000-4-2, criterion B JEDEC JESD22-A114-B Human Body Model
Laser Safety	21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3. described in Laser Notice No. 56, dated May 8, 2019.
Environmental	RoHS 10 (2011/65/EU + 2015/863) ISA S71.04 G2

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

11 REFERENCES

1. IEEE - “802.3bs-2018”
2. QSFPDD MSA - “QSFP-DD Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVE Rev. 5.1”
3. QSFPDD MSA - “QSFP-DD Management Interface Specification Rev 4.0”

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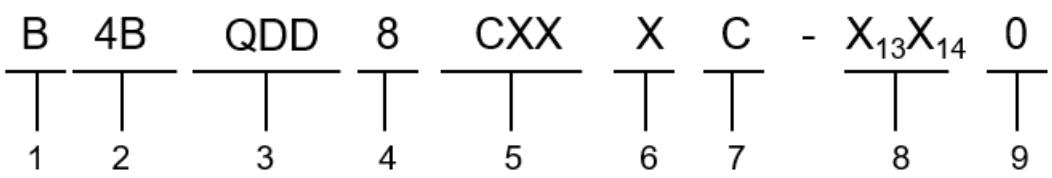
12 ORDERING INFORMATION

Table 11 Product Code



Item	Parameter	Symbol
1	Product Category	B
2	Data rate	4B: 400G
3	Module Form Factor	QDD: QSFP-DD
4	Channel (TX)	8: 8CH
5	Distance	C: AOC, XX: Length in meter (01: 1m, 03: 3m, 05: 5m, 07: 7m, 10: 10m, 20: 20m, 100:100m)
6	Connector Type	X: AOC
7	Operating Temperature Range	C: 0~70C
8	Customer Code	XX: Standard Product
9	Revision	0

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13 REVISION HISTORY

Rev.	Date	Note
1.0	2023/06/20	New released
1.1	2024/04/08	Change label dimension

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